ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	METHOD FOR SEPARATELY OPTIMIZING THIN GATE DIELECTRIC OF PMOS AND NMOS TRANSISTORS WITHIN THE SAME SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED THEREBY

Application Number :

Confirmation Number:

First Named Applicant: Anthony Chou

Attorney Docket Number: FIS920030228US1

Art Unit:

Examiner:

Search string: (6093661 or 6417546 or 6541395 or 6451662 or 20030082884 or 20020130377 or 20030100155 or 20030027392).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6093661	2000-07-25	Trivedi, et al.			
	2	6417546	2002-07-09	Trivedi, et al.			
	3	6541395	2003-04-01	Trivedi, et al.			
	4	6451662	2002-09-17	Chudzik, et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20030082884	2003-05-01	Faltermeier, et al.			
	2	20020130377	2002-09-19	Khare, et al.			
	3	20030100155	2003-05-29	Lim, et al.			
	4	20030027392	2003-02-06	Gousev, et al.			

Signature

Examiner Name	Date